AMENDMENT TO THE CLAIMS

1. (Previously Presented) An apparatus comprising:

an internal test bus (ITB);

a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller;

an integrated test controller (ITC) coupled to the ITB, said ITC having an instruction register and a test access port finite state machine (TAP FSM); and

a debug unit coupled to the ITC, said debug unit triggers a signal as an input to said ITC in response to an externally generated test signal;

wherein the ITC only generates a single global control signal and each of the deskew controllers generates a first local control signal and a second local control signal in response to the single global control signal, where said ITC encodes and transmits states of said TAP FSM and test instructions to at least one logic unit controller over said ITB to test said apparatus, wherein a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction.

2. (Previously Presented) The apparatus of claim 1, wherein each of the plurality of deskew clusters further comprise a plurality of deskew buffers and a regional clock driver (RCD).

3. (Previously Presented) The apparatus of claim 1, wherein the single global control signal and one of the first local control signal, the second local control signal, and both the first local control signal and the second local control signal provide a distributed test control scheme for integrated circuits including debug and testability operations.

4. (Previously Presented) The apparatus of claim 1, wherein the first local control signal is a snapshot instruction and the second local control signal is a shift instruction.

5. (Original) The apparatus of claim 4, wherein a snapshot instruction can be issued at a first time period and a shift instruction can be issued at a second time period, and results from the snapshot instruction can be shifted by the shift instruction after a third period of time.

6. (Currently Amended) A method comprising:

generating a single global control signal in an integrated test controller within an integrated circuit in response to an external signal;

decoding the single global control signal in a deskew controller in the integrated circuit;

generating a first local control signal corresponding to the single global control signal;

distributing the first local control signal to a regional clock driver (RCD); and

performing one of a debug operation and a testability operation on the integrated circuit by using the single global control signal and the first local control signal, where a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction.

7. (Previously Presented) The method of claim 6, further comprising generating a second local control signal corresponding to the single global control signal.

8. (Previously Presented) The method of claim 7, wherein one of the first local control signal is a snapshot instruction and the second local control signal is a shift instruction.

9. (Original) The method of claim 8, further comprising issuing a snapshot instruction at a first time period;

issuing a shift instruction at a second time period; and shifting results from the snapshot instruction by the shift instruction after a third period of time.

10. (Original) The method of claim 6, further comprising triggering the debug operation after a variable time period.

11. (Currently Amended) A program storage device readable by a machine comprising instructions that cause the machine to:

generate a single global control signal in an integrated test controller within an integrated circuit;

decode the single global control signal in a deskew controller within the integrated circuit;

generate a first local control signal corresponding to the single global control signal;

distribute the first local control signal to a regional clock driver (RCD); and

perform one of a debug operation and a testability operation on the integrated circuit by using the single global control signal and the first local control signal, wherein a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction.

12. (Previously Presented) The program storage device of claim 11, wherein the instructions further cause the machine to:

generate a second local control signal corresponding to the single global control signal.

13. (Previously Presented) The program storage device of claim 12, wherein the first local control signal is a snapshot operation and the second local control signal is a shift operation.

14. (Original) The program storage device of claim 13, wherein the instructions further cause the machine to: issue a snapshot operation at a first time period;

issue a shift operation at a second time period; and shift results from the snapshot operation by the shift operation after a third period of time.

15. (Original) The program storage device of claim 11, the instructions further cause the machine to: trigger the debug operation after a variable time period.

16. (Currently Amended) A system comprising:

at least one processor;

a global bus coupled to the at least one processor;

a memory coupled to the global bus;

an internal test bus (ITB) located within the at least one processor;

a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller;

an integrated test controller (ITC) coupled to the ITB; and

a debug unit coupled to the ITC;

wherein the ITC only generates a single global control signal and each of the deskew controllers generates a first local control signal in response to the single global control signal to test the at least one processor, wherein a snapshot instruction and a shift instruction are partitioned into separate operations, and it is not necessary to synchronize the snapshot instruction and the shift instruction.

17. (Previously Presented) The system of claim 16, wherein each of the plurality of deskew clusters further comprise a plurality of deskew buffers and a regional clock driver (RCD).

18. (Previously Presented) The system of claim 16, wherein each of the deskew controllers further generates a second local control signal, wherein the single global control signal and one of the first local control signal, the second local control signal, and both the first local control signal and the second local control signal provide a distributed test control scheme for integrated circuits including debug and testability operations.

19. (Previously Presented) The system of claim 16, wherein the first local control signal is a snapshot instruction and the second local control signal is a shift instruction.

20. (Previously Presented) The system of claim 19, wherein a snapshot instruction can be issued at a first time period and a shift instruction can be issued at a second time period, and results from the snapshot instruction can be shifted by the shift instruction after a third period of time.